

a first SOG layer, which is formed in side surfaces of said dummy pattern and said first insulating layer;

a second SOG layer, which is formed on a top surface of said dummy pattern and said first SOG layer, said second SOG layer being denser than said first SOG layer; and

a second insulating layer, which is formed on said second SOG layer, wherein said first and second insulating layers and said first and second SOG layers are exposed at a boundary between the first region and the second region.

20. (Newly Added) A semiconductor memory device as recited in claim 20, wherein the memory device is a DRAM.

21. (Newly Added) A semiconductor memory device as recited in claim 20, further comprising a redundant circuit having a redundant memory cell.

22. (Newly Added) A semiconductor memory device as recited in claim 20, further comprising a plurality of laser blown fuses.

Remarks

Status of the Claims

Upon entry of the present amendment claims 1-22 are pending in the present application. Claims 1-9 were previously withdrawn from consideration. Of the pending claims, claims 10, 13, and 19 are independent. Claims 19-22 are newly added. Support for these newly added claims may be found in the description of the third preferred embodiment on page 13 of the application as filed.